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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/986,789	11/09/2001	Toshiaki Ito	027260-501	5975

7590 02/01/2005

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EXAMINER

PALADINI, ALBERT WILLIAM

ART UNIT	PAPER NUMBER
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2125

DATE MAILED: 02/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/986,789	Applicant(s) ITO ET AL.	
	Examiner Albert W Paladini	Art Unit 2125	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 November 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-18 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>1/30/02</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 1-18 are rejected under 35 U.S.C. 102(a) as being anticipated by Applicant's cited prior art in figure 30 of the specification.

Applicant's recited prior art in figure 30 discloses the information merging section 103, the connection information section 104 for generating connector information between the lead frame and semiconductor chips, an integrating section 106 for generating integrated connection information between the semiconductor chips and the lead frame from the connection information provided by section 104. The title of section 106 "COMPLETE CONNECTION DIAGRAM STORING SECTION" teaches that the entire connection information may be displayed on a single drawing.

Relevant Prior Art

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Akasaka (4989166) discloses a method for the design of a mold for a semiconductor plastic package with a semiconductor chip with a mounted lead frame. The invention further includes model interaction synthesizing means for dividing the shape by interaction processing, defining the amount of a feature in an interactive manner and allocating

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an analysis model to a partial shape, log retaining means for retaining input information during interactive processing, know-how forming means for registering know-how in the know-how registration means from log information to form a know-how effective for synthesizing models, and know-how editing means for merging know-how already registered in the know-how registration means and know-how formed by the know-how forming means and avoiding an occurrence of contradiction between the different know-how.

Ogawa (6349240) disclose a semiconductor device manufacturing system including chip and related lead frame information, including relevant coordinate positioning. Chip failure information is merged with wafer test information in order to obtain a complete distribution of failure history.

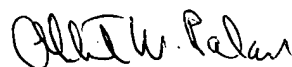
Akram (6762502) discloses a method of forming semiconductor device packages where before fabrication of an object, the files for the support and the structure are merged. This includes chip and associated lead frame information.

4. Any inquiry concerning this communication or earlier communication from the examiner should be direct to Albert W. Paladini whose telephone number is (571) 272-3748. The examiner can normally be reached from 7:30 to 3:30 PM on Monday, Tuesday, Thursday, and Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Leo P. Picard, can be reached on (571) 272-3749. The official fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

January 31, 2005


Albert W. Paladini
Primary Examiner
Art Unit 2125